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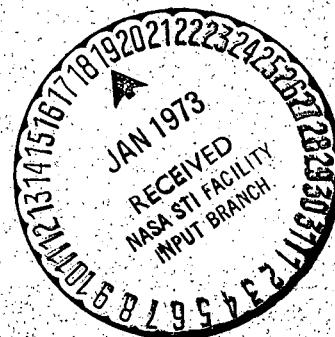
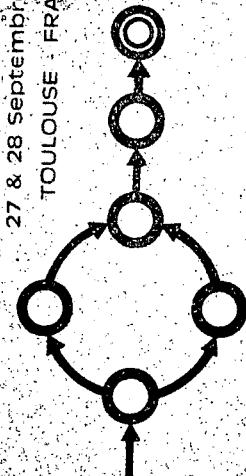
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# Conception et Maintenance des Automatismes Logiques

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## A UNIVERSAL FUNCTIONAL OBJECT

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**ABSTRACT:** This paper presents a scheme for realizing any function, combinational or sequential, in a single universal function scheme, termed the universal function object UF. This universal functional scheme is addressed to the problem of the proliferation of the number of parts (cards, chips) necessary for conventional implementation in an LSI technology of a computer system (terminal, or peripheral systems). A UF implementation would use only one or a few, the various specializations being effected by insertion of the appropriate "connection vector". To use the universal functional scheme of implementation, the designer would proceed in conventional manner to produce a conventional design; a simple program would then faithfully translate this into a UF design. The UF implementation will use about ten times more circuits than a conventional implementation, regardless of the size of the design. However, there will be only one (or a few) distinct cards to form, so that actual manufacturing and stocking costs should be drastically reduced. Another feature of the UF approach is the following. Suppose that a particular circuit in the UF has failed, which fact we would have detected and diagnosed by precomputed and stored tests [4]. Then we have "general-purpose spares" and, by means of a new connection vector cv, logically disconnect the failing circuit, appropriately a connect spare properly biased by cv, thus substituting for the failing circuit. This procedure could be used both at manufacture, to increase the yields, as well as in the field, to achieve automatic repair. This work was supported in part by the Jet Propulsion Laboratory, California Institute of Technology, under the National Aeronautics and Space Administration Contract NAS-7-100.

In a recent disclosure I showed [1] how to realize any (finite) function, sequential or combinational, by means of a single type of primitive functional object, essentially by appropriately assigning values to strategically placed memory elements which constitute a part of this primitive, called a universal functional element UF.

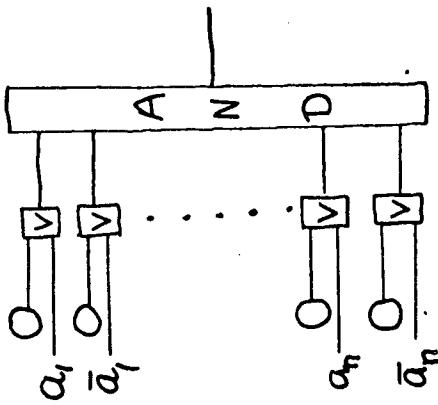
For combinational functions, this type of implementation utilized, however, only two levels of logic, at least in its most literal interpretation. For some functions, such as the parity-check function of any substantial number of variables, this might be a prohibitively costly method of implementation, although a way around this particular function, the parity-check, was given in [1].

This first extension given here removes the limitation to two levels to the UF; it allows, just as does ordinary "fixed-logic" implementation, many levels of logic in any given form of implementation. It extends directly to the sequential case, in which case loops (controlled) are introduced.

It appears at this stage in the development of these ideas that actual large-scale logical design using UF's will most expeditiously be done by having a variety of UF's, of differing size and complexity, in spite of the fact that any one sufficiently large UF type would suffice for any job - it is a matter of efficiency.

The second extension in this note addresses itself to the repairability of the universal functional object UF. We shall consider first the combinatorial case implemented in two levels the general scheme is shown in Figures 1 and 2.

It is also clear how Engineering Changes ED's, corrections or improvements to the design, can be effected merely by a change to the connection vector: no hardware scapping, the ED's simply effected and tested out.



Here the individual circles represent bits of memory, possibly arranged in shift-register style:

if for a given input  $a_i$ , it is desired that  $a_i$  be ANDed in this universal AND, then the corresponding memory element feeding the OR-block, which  $a_i$  also feeds, is made equal to 0. If not, then the contacts of this memory element is made equal to 1, suppressing thereby the  $a_i$ . Similarly one treats the complementary variable  $\bar{a}_i$ . If it is desired that neither  $a_i$  nor  $\bar{a}_i$ , feed this AND then the memory bits of each is set equal to 1.

Figure 1. The Universal AND block UA

Let us take a few examples to see how we would design logic in this two-level or, as we prefer to call it, one-stage method.

That on the right is a 4-input 3-output function. The symbol  $x$  on the left means that with the other variables at the specified values, the output described on the right will be maintained regardless of the values assigned to the input variables having the value  $x$ . On the right of the vertical line, the output side, an  $x$  means that that term is not to feed that particular output [2]. IBM System 360 Program MCW exists to minimize the number of these rows (cubes) for any given (multiple-input, multiple-output) function [3].

a	b	A	a	b	c	d	B	C	D
1	0	1	1	0	1	x	1	x	1
0	1	1	x	x	0	0	1	1	1
			1	1	x	1	x	1	1
			0	0	1	1	x	x	1

exclusive-or

some other function

#### Automatic-Repair on the Universal Function Object

Before we describe the case when the function is sequential (hence has memory) we describe a simple means of using the UF so as to be able in effect to remove or disconnect failing logic elements of the UF and to codify spare general-purpose elements on the UF and to connect it, again by purely logical means, so that it performs precisely the function formerly done by the failing element.

The exclusive-or is implemented for the universal element as shown in Figure 3.

Figure 2. Tabular or cubical description of two functions.

In Fig. 2, the function on the left is the exclusive-or, with inputs  $a$ ,  $b$  and output  $A$ .

Tests to detect and diagnose failures can be computed by the D-algorithms with particular ease because of the great control over each logical element.

Imagine then that we have  $n$  active Universal AND blocks and along with these general-purpose spares "floating", i.e. not contributing to the outputs; see Figure 5.

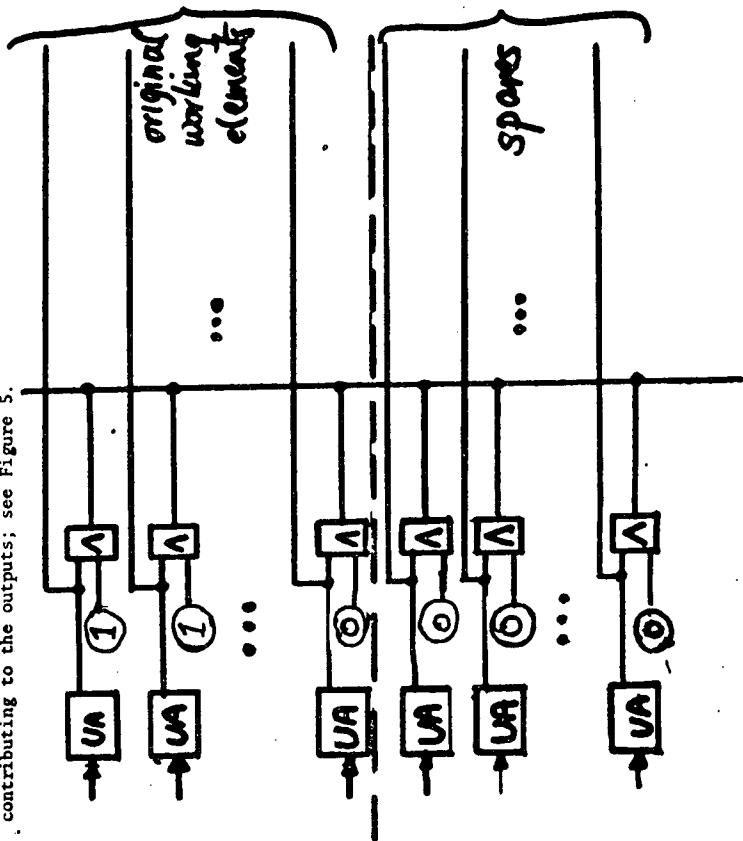


Figure 5. UF with general-purpose spares

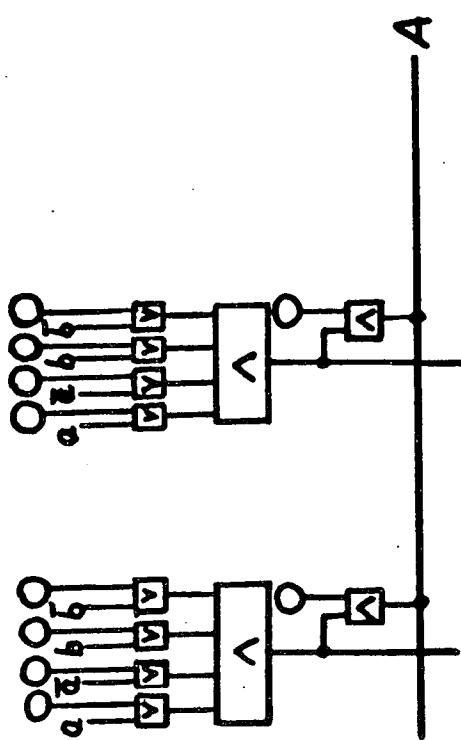


Figure 3. UF Implementation of exclusive-or.

Originally the  $r$  general-purpose spares are switched off, which condition can be achieved, for example, by setting the memory elements for the output contact equal to 0.

the same replacement scheme could be to "repair" any faulty "B-logic". We show this by the following diagram and argument.

Suppose then that one of the original working elements is found to be malfunctioning, e.g. by application of a complete set of tests ("complete" means giving 100% coverage).

Thus, this element must be switched out which is done, as above, by setting all of its memory elements for its outputs to 0.

Second, the connection vector which this universal and block had, i.e. the pattern of its memory bits controlling its input configuration, must be impressed into the similar memory bits for the spare selected for this replacement operation. Likewise the pattern of the memory output connections must similarly be duplicated.

Clearly this replacement scheme can be continued until all the spares are used up. It is worth noting that this procedure could be used in the manufacturing process, so that a given part need not be perfect - only a sufficient number of them. This would raise the yield.

Suppose that we call the output variables from the first stage (two levels of logic) B. Then if, as we shall discuss shortly, the 3 variables were used as inputs to subsequent stages of logic precise

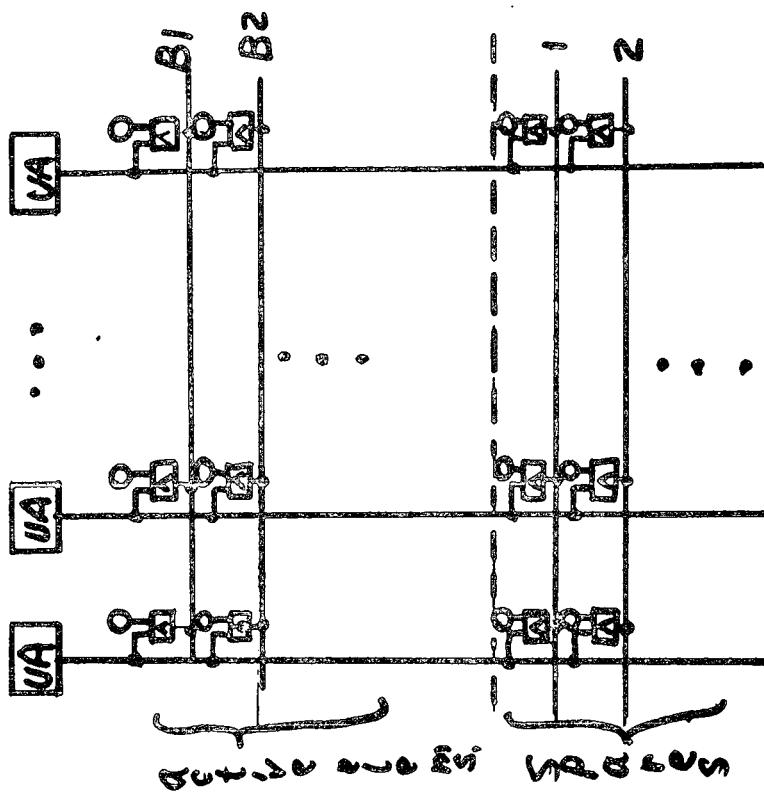


Figure 6. Illustration of operation of replacement of one of the outputs of the first stage.

We refer to the figure: If  $B1$  should fail, then it would be logically disconnected and spare  $1$  would be invoked to serve as its substitute, with the outputs from the first stage made the same for the spare as for the line  $B1$  which it is replacing.

We would then have  $z$  stages in the Universal Functional Object UF appropriately biased; note that there may be several levels of logic within each stage. In the interest of simplicity rather than draw a general circuit for the above functional expression, we will give two detailed examples of UF - implementation, namely a four-bit parity check circuit and an adder of two two-bit numbers.

Note: if in the second stage (and similarly for later stages)

It were desired that  $\overline{B1}$ , the complement of  $B1$ , be an input to some vertex function, say an AND, this could easily be achieved by including a negation complement with  $B1$  as an input. It could also be achieved, however, by

Observing that, if the outputs to  $B_1$  are denoted as  $b_1, \dots, b_k$ , then  $b_1 = b_1 \vee b_2 \vee \dots \vee b_k$ , so that  $\bar{B}_1 = (b_1, b_2, \dots, b_k)$ ; thus if a NAND function is provided,  $\bar{B}_1$  can be easily provided, and independently from the function  $\bar{B}_1$ .

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Note: a failure in the memory cell could equally well be considered as a failure in the appropriate logic block and treated, by replacement, in the same manner as any failure of the logic block.

Take now a function which is implemented in a library

$b = B(a)$   
 $c = B(b, a)$   
 $d = D(c, b, a)$   
 $\vdots$   
 $z = Z(y, \dots, a)$

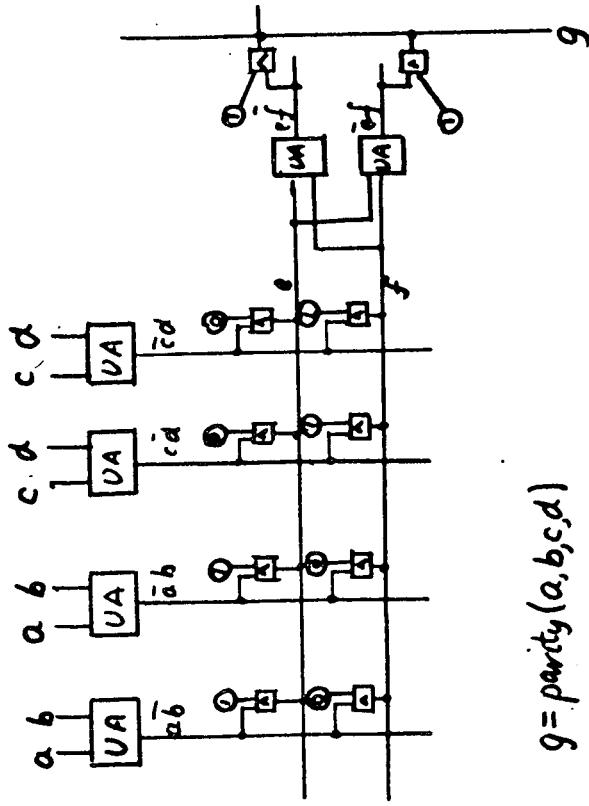


Figure 7. UF -Implementation of a 4-bit parity check circuit.

Fig. 9 is a straight-forward implementation of a two-bit adder. It may be seen that this implementation uses three exclusive-or's and two AND's both of which we have given UF implementations.

first bits	second bits	$A$	$B$	$C_i$	$S_i$	$C_o$
0 0	0 0	0	0	0	0	0
0 1	1 0	0	1	0	1	0
1 0	0 1	1	0	0	0	1
1 1	0 1	1	1	1	1	1

first bits	second bits	$A$	$B$	$C_i$	$S_i$	$C_o$
0 0	0 0	0	0	0	0	0
0 1	1 0	0	1	0	1	0
1 0	0 1	1	0	0	0	1
1 1	0 1	1	1	1	1	1

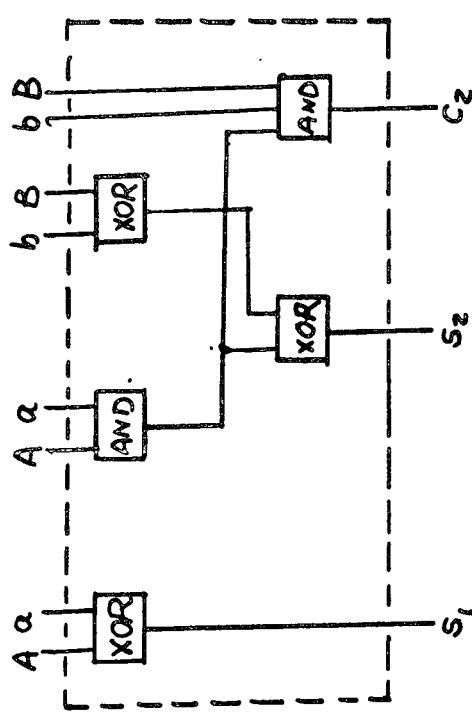


Figure 8. Function table for a 2-bit adder.

Figure 9. Standard implementation of a 2-bit adder.

We have seen how to implement each of these functions, AND and XOR are implemented on a UF; for the sake of completeness, however, we shall make an explicit UF-implementation.

In this picture not all of the memory cells and other lines are shown: only enough so as to exhibit the scheme clearly.

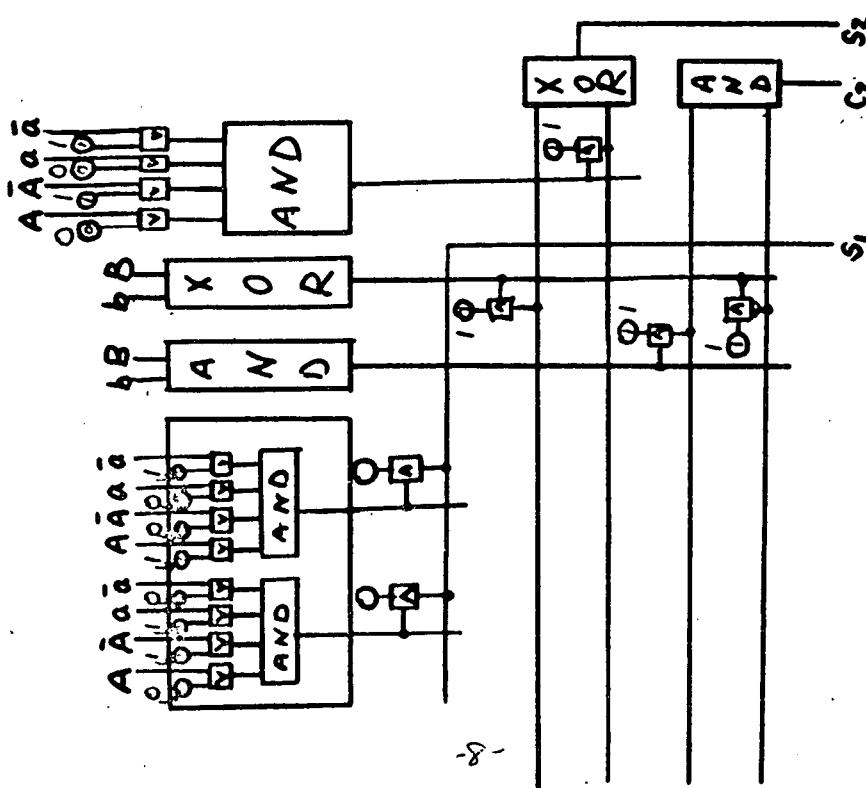


Figure 10. Translation of adder implementation of Fig. 9 into a UF-implementation.

The scheme for having memory or feedback is very simple. Imagine a line  $y$  emanating from say the first stage of implementation and that it is desired, possibly upon appropriate delay or arrival of a timing pulse, to feed this signal back to the input of this stage. Then  $y$  is fed into an AND block together with a memory element, say  $m$ . If it is desired that  $y$  be fed back and hence its value "remembered" then  $m$  is set to 1; otherwise 0. Then the output of this AND - call it  $y^*$  - is then fed into an OR whose other input is a primary input  $p$ . When  $y = 0$  then clearly  $p$  is transmitted through the OR-block so that with respect to this line at least the circuit is behaving combinationally. When, however,  $m = 1$  then  $p$  is set to  $C$  and  $y$  comes through the OR. This is the basic scheme as described in [1].

If input lines to the AND's in the first stage are at a premium, one might use the following selection scheme.

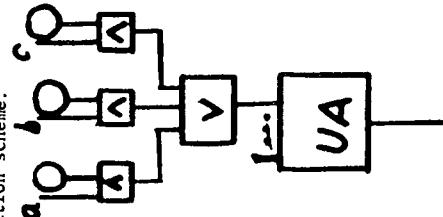


Figure 11.

Here we indicate a particular input line to the Universal AND block and here any of the inputs  $a, b, \dots, c$  may be selected, in general exactly one of them, by appropriate selection of its characteristic value: 1, 0, ..., 0 or 0, 1, 0, ..., 0, ..., or 0, 1.

This device can mitigate against the building up of an excessive number of inputs to the UA's.

In general each stage would have a suitable number of designated output lines which could be feedback lines. Selections could be made among these along the following lines.

-9-

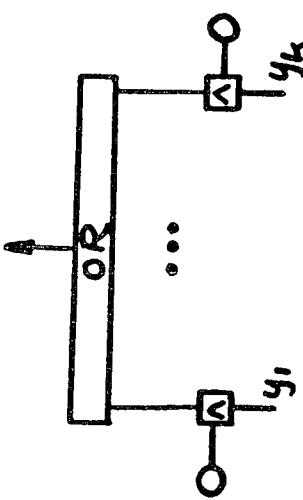


Fig. 12. Selection for feedback among the outputs of a given stage with the memory contents being 1, 0, ..., 0 or 0, 1, 0, ..., 0 or 0, ..., 0, 1.

It would probably be infeasible to have one or more output lines going from each stage  $i$  back to stage  $i - 1$  and one could easily cascade back stage-by-stage although for fast applications this might be unacceptable.

REMARK: it is clear than an Engineering Change can be effected by changing the connection vector for the affected UF ; this will greatly reduce the cost effecting engineering changes.

Remark: It is quite straightforward to transform any simplex or ordinary logic design into a UF -design which is "isomorphic" to the simplex design in the sense that when the connection vector is appropriately assigned the various levels and gates of the original design can be seen in the UF -design and vice versa. In fact one could write a program to effect such a transformation.

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#### Section 5. MIN360

One of the first problems encountered by designers of switching systems was that which is called today minimization of two-level realizations. In its original form it was concerned with the minimization of contacts in "strict series-parallel" form. Manual procedures were developed, by Karnaugh, Quine and McCluskey, the latter being adapted to digital computation, for small problems at least. In their original formulation the problem was for a single output function, that is to say, the minimization in normal form of a single output function. Concrete problems, however, usually have many outputs. A typical problem would be a two-level circuit transforming from one code to another. This inherently is a multiple output problem. A geometric method, designed for digital computation, was described in RC-11. This was programmed in a series called MINI through MIN6 over the period 1958 to 1961. It was adapted early using a scheme due to Muller for multiple outputs. It could not be guaranteed the multiple output form, however, to obtain a minimum solution. Various approximations were incorporated into the program, for example MAP, standing for Minimum Approximate. This program proved to be highly useful on problems out of the range of the strict minimization procedure. The MIN system of programs received extensive usage within IBM. (RC 1425).

In 1966, the Jet Propulsion Laboratory, in response to its needs for two-level realizations made a search, which the aid of IBM, for a decent minimization program. MIN 6 was tried and as a result of

experiments modified so as to be more convenient for JPL usage. As a result of this renewed interest in minimization, we became interested again in the two-level multiple-output minimization problem, and using a different representation for cubes - singular cubes - we were able to extend the extraction algorithm to the multiple output case. (RC 2007, 2280) This algorithm was first programmed in APL and proved out very small problems. It was then reprogrammed by Leroy Junker in PL/I with assembler language subroutines and run on the Model IBM System/360 Model 91.

In addition new approximate procedures and options were developed. For example, for Functional Memory the appropriate cost function is not the classical one, the number of input lines, plus the number of output lines, but rather the total number of cubes in the cover - this would correspond to the number of words in the Functional Memory realization of the function.

We will now describe how the program may be used in its various options; for simplicity we will call MIN360 by the abbreviated name MIN.

First let us describe the input format, which is the same as the output format. Suppose that we have a function of  $r$  binary inputs and  $s$  binary outputs. The cubical cover is a description of the input-output relations for this particular function. One mode of

description, for example, would be to list all  $2^r$  input patterns with their corresponding outputs if any. For  $r$  large this may not be practically possible. For functions of large numbers of variables, it is most often the case that relatively few combinations of the input will determine the output. Suppose for example that the first  $p$  of the inputs, if all 1, will cause each output to be 1. This would be represented as a string of  $p$  1's followed a string of  $r-p$  x's followed by a vertical slash followed by  $s$  1's. The minimization algorithm MIN360 is a function of the care conditions the don't-care conditions the mode, which will be explained, the cost function, a cost bound and truncation number. Thus we may write the solution  $s = \text{MIN360}(c, d, mode, bound, truncation)$

The care conditions  $c$ , don't-care conditions  $d$ , have already been described. The mode may be EXACT, meaning that a minimum will be obtained; PSEUDO meaning that a simplification of the algorithm will be used; in PSEUDO, after an extremal is computed it is thrown entirely into the developing solution  $s$ , whereas in the exact solution only that portion thereof which contains distinguished vertices may be thrown in. This procedure hastens the computation of a solution. After a solution is obtained, redundant outputs are removed. This is similar to the MIN6 mode for multiple outputs. Although it is in general faster than EXACT, the solution cannot be guaranteed to be a minimum. We ran a JPL problem for 2 hours in the EXACT and the PSEUDOMode; the EXACT mode obtained a solution of cost 409, whereas for the PSEUDOMode, the

cost was about 427.

As indicated the cost function varies from one technology to another; the classical cost function counts the number of 1's and 0's in the input part of the cube in the solution and the number of 1's in the output. If one were to design a two-level AND-OR realization this would be the appropriate cost.

With the costbound option, cbound, if one assigns a costbound  $k$  to the developing solution, as soon as  $k$  is exceeded that part of the search is terminated. Under the truncation option, one assigns a number  $t$  and as soon as the branching level exceeds  $t$ , the computation ceases: one uses whatever solution or solutions of those computed up to that point.

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The mode may take on the values EXACT, PSEUDO and APPROX. We will now explain APPROX. First a word, however, about the exact minimization procedures. For very large problems it is frequently the case that "branching" occurs. This means that a decision tree must be examined, each node of which involves, in general, considerable computation. Thus, as the size and complexity of the problem to be solved increases, the running time for the program correspondingly increases. Since we are interested in solving quite large problems - the data format for the program allows problems having up to 32 inputs and 32 outputs - it is important to have an APPROXimation which will get an

answer hopefully close to a minimum, and in a reasonable, preferably very short, amount of time.

The APPROXimate procedure starts, as all MIN options, with a cover  $C$  of all input conditions for which an output should be 1: this is referred to as the ON-array; also either a cover of the DON-T-CARE's, i.e. input conditions together with those corresponding output conditions for which one does not care or is indifferent to the corresponding output or else a cover of the OFF-array i.e. a cover of input conditions or patterns for which some outputs are zero. For example, for 3 inputs and 2 outputs one might have

C, ON-array =	inputs		outputs	
	input	output	input	output
	1 x 0	1 x	1 0 1	1 1
	x 1 1	x 1		
	0 0 0	1 1		

1. The first step of the algorithm is to take the first cube of the ON-array, in our example  $1 \times 0 \mid 1 \times$  and a coface of the first coordinate, i.e. change the first coordinate to an  $x$  if it is not already  $x$ . Then one "sharps" away the cubes of the cover; the  $\#$ -product is a procedure for finding, for a and b cubes, a cover of the set of all vertices of a that are not contained in b. If C is a set of cubes then  $a \# C$  is an iterated product of a with all cubes of C. See RC 2008 for details and an explanation.

If the  $\#$ -product of the cofaced cube  $a$  of the initial cover and the initial cover  $C$  and  $D$  is empty, then changing this coordinate to an  $x$  is a valid step and  $a$  is replaced by the larger cube (in general covering more) and the procedure is repeated for each input coordinate of  $a$  which is not  $x$ . After this is completed, each output coordinate which is  $x$  is changed provisionally to a 1 and again the  $\#$ -product of the cube modified, with the original covers  $C$  and  $D$  is used to ascertain whether or not this change is valid; this modification is done again for each output coordinate, one after the other. This cofacing operation is done for each cube of  $C$ ; call the result  $E$ .

2. The second step ascertains if any cubes of  $E$  are redundant.

This is done by performing for each cube  $e$  of  $E$  the test

$$\frac{1}{e} \# ((E - e) \vee D.)$$

If the product is  $\emptyset$  then  $e$  is redundant;  $e$  is then removed from

E. This procedure is applied to every cube of  $E$ ; this process produces a cover  $F$  which is irredundant, i.e. no cube can be deleted and still remain a correct expression of the original function.

3. The third step is to ascertain if any output coordinates of cubes of  $F$  are redundant. This is done by changing, in a given cube with respect to a given output coordinate which is 1 for this cube, all other output coordinates, which are 1, to an  $x$  and forming from that the  $\#$ -product with all other cubes of the cover  $F$  plus the Don't-care

cover  $D$ . If this product is  $\emptyset$  (empty) then this particular output coordinate is redundant and may be removed, i.e. changed to an  $x$ . The process is performed for every output coordinate whose value is 1 for every (singular) cube of  $F$ . The resulting cover,  $G$ , is an irredundant prime-cube cover and, experiment by computer shows, gives covers whose cost, being the number of cubes in  $G$  in many applications, is remarkably near to a minimum.

In fact for large problems, say in excess of 12 inputs and 12 outputs, we will inevitably use this APPROX mode. The previous quarterly report gave running times for the computation on IBM System 360/91 of minimum covers, for approximate minimum covers, for a fairly wide range of problems, several of them being problems originating with M. Perlman at JPL. A manual for MIN360 is under preparation and will be sent to JPL upon its completion.

## Section 6. Diagnosis of Failures in Mechanisms

Consider any component of a mechanism  $M$ . Assume that its "state" - position, velocity, pressure, tension, . . . - can be characterized by a quantum number, assumed with no loss of generality to be in binary form,

of bounded length. The state of a component  $c$  is a function of the

"output states" of certain other components of  $M$  which directly affect it, plus possibly its own "previous" state. For simple  $c$  this function may be expressed as a function-table or function-ensemble of function-

pairs. The component function-tables constitute a computable characterization of the function or behavior of  $M$ . Essentially  $M$  is treated as a physical, mathematical interconnection of its components.

A "failure" of a component  $c$  is any change which modifies the function it performs; a failure of  $M$  is a failure of any of its components. Primary

Inputs  $P_1$  of  $M$  are those output states or variables of mechanisms outside of  $M$  which determine the functioning of  $M$  given its structure. Primary

Outputs  $P_0$  are those output states of  $M$  which are measurable and perceptible outside of  $M$  and are the result of  $M$ 's functioning.

A test  $T$  for failure  $F$  of  $M$  is a (sequence of) Primary Input patterns such that the corresponding  $P_0$  pattern differs depending upon whether or not  $F$  has occurred. Problem: given a failure in  $M$ , find a test to detect it. It does not appear difficult in principle to adapt the D-calculus (quantum calculus) to this model of the functioning behavior and failure diagnosis of mechanisms. The hard part is to provide this functional description of a mechanism whose design may be recorded at

best by conventional drawings, further to be able to do this in a Design-Automation mode. Also there is the problem of characterizing and describing the behavior of components subject to a particular failure.

Nevertheless it seems an approach novel to mechanical diagnostics is being pursued actively.

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